

PTO/SB/088 (08-03)

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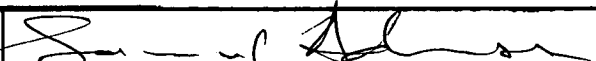
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Application Number	10/033,716
Filing Date	12/28/2001
First Named Inventor	Robert W. Bower
Art Unit	8633
Examiner Name	S. A. Gebremariam
Attorney Docket Number	BOW5075.04A

Sheet 1 of 1

NON PATENT LITERATURE DOCUMENTS

Examiner Initials ¹	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
R		Ellis, R. K. et al. "Electron Tunneling in Non-planar Floating Gate Memory Structure", IDEM, 1982, pp. 749-752.	
R		Shealy, J.R. et al. "Direct band gap structures on nanometer-scale, micromachined silicon tips", Appl. Phys. Lett. Vol. 70, No. 25, June 1997, pp. 3458-3460.	
R		Prickett, B.L. et al. "Trapping in Tunnel Oxides Grown on Textured Polysilicon", 21st annual Proceedings on Reliability Physics, 1983, pp. 114-117.	
R		Dimitrijević, S. "Understanding Semiconductor Devices", Oxford Press, New York, ISBN 019513186X, 2000, Chapter 8, Photonic Devices, Fig. 8.10.	
R		Neamen, D. "Semiconductor Physics & Devices - Basic Principles", second edition, ISBN 0256242143, 1997, p. 67.	
R		Mayer, J.W. "Electronic Materials Science: For Integrated Circuits in Si and GaAs", Macmillan Publishing, ISBN 0-02-378140-8, 1989, Section 14.8, pp. 431-436.	
R		Grove, A.S. "Physics and Technology of Semiconductor Devices", John Wiley and Sons, ISBN 0471329983, 1967, pp. 128-129.	
R		Sze, S.M. "Physics of Semiconductor Devices", Wiley-Interscience, ISBN 0471056618, 1981, pp. 46, 47, 690, 691.	
R		Wegener, H.A.R. et al. "The prediction of textured poly floating gate memory endurance", 23rd annual Proceedings on Reliability Physics, 1985, pp. 11-17.	

Examiner Signature		Date Considered	7/7/04
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